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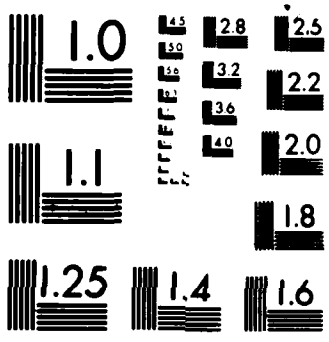

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Air as an Adjustable Insulator for C-V and G-V Analysis of Semiconductor Surfaces

by

John Moreland, Jeff Drucker, P. K. Hansma, Jörg P. Kotthaus
Arnold Adams and R. Kvaas

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Department of Physics (JM, JD, PKH)
University of California
Santa Barbara, CA 93106

Institute für Angewandte Physik (JPK)
Universitat Hamburg
West Germany

Santa Barbara Research Center (AA, RK)
Goleta, CA 93117

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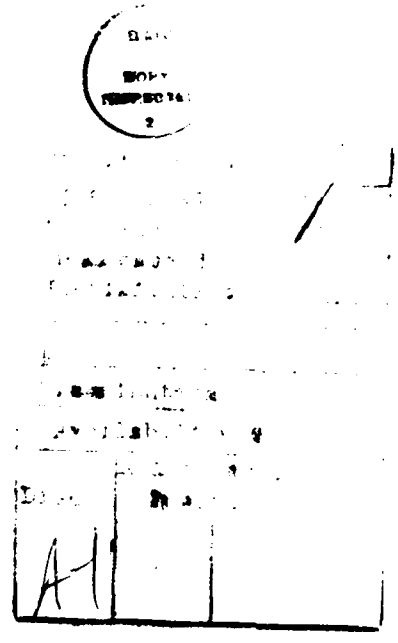
John Moreland, Jeff Drucker and P. K. Hansma
Department of Physics
University of California
Santa Barbara, CA 93106

and

Jörg P. Kotthaus
Institut fur Angewandte Physik
Universitat Hamburg
Jungiusstrasse 11
200 Hamburg 36
West Germany

and

Arnold Adams and R. Kvaas
Santa Barbara Research Center
75 Coromar Dr.
Goleta, CA 93117



ABSTRACT

An adjustable metal-air-semiconductor capacitor was fabricated using a Pb disk suspended 1700 - 3600 Å above an n-type Si <111> surface. Experimental differential capacitance versus voltage and differential conductance versus voltage curves are similar to those previously obtained for metal-oxide-semiconductor capacitors.

Metal-insulator-semiconductor (MIS) capacitors have been an integral part of the rapid growth of semiconductor technology. Their applications include surface characterization, transistor technology, charge coupled devices and solar energy.[1-4]

The fabrication of these capacitors relies on the formation of a natural or deposited insulating barrier between a metal electrode and the semiconductor surface. The natural oxide of Si forms a uniform insulator well suited for MIS experiments.[5] Deposited insulators are used with other materials.[6]

Often, however, it is necessary to determine the effects of such insulators on the electrical characteristics of the capacitors before the semiconductor physics can be understood. For example, mobile and fixed charges in an oxide insulator alter the response of a semiconductor surface to an externally applied electric field. In addition, insulator formation changes the semiconductor surface making measurements that may be valuable to the understanding of surface chemical processes impossible. Ideally, a metal electrode suspended above the semiconductor surface forming a distinct vacuum or air insulating gap would overcome these limitations. The gap should be mechanically stable and uniform to within a few nm to insure constant fields at the semiconductor surface as is the case for natural and some deposited insulators.

We present here a promising technique for constructing air-gap MIS capacitors that may satisfy these requirements. It has been used to make mechanically adjustable tunneling

barriers stable at approximately 10 Å to within ± 0.1 Å.[7,8] Preliminary measurements on a Pb-air-n type Si <111> capacitor are also presented using the differential capacitance versus voltage method pioneered by Terman[9] and developed by Lehovec and Slobodsky[10] and the differential conductance versus voltage method developed by Nicollian and Goetzberger.[11]

A MIS capacitor of the type described above is illustrated in Fig. 1. A 9 μm thick metal electrode evaporated on a 1 mm thick glass microscope slide is supported above a polished semiconductor surface by 10 μm evaporated spacers so that a 1 μm air-gap exists between the metal and semiconductor. The gap is compressed using an electromagnetic squeezer that flexes the microscope slide along a 5 mm diameter ring centered about the 1 mm diameter electrode.[8] Electrical connection is made to the metal electrode by 1 cm long, 0.1 mm wide, 0.1 μm thick evaporated leads. This geometry insures a background capacitance of a few picofarads, a small fraction of the total capacitance when the capacitor is compressed.

Pb-air-n type Si <111> capacitors in this configuration were constructed using carefully cleaned substrates in a laminar flow hood that enclosed the opening of the vacuum chamber to minimize dust. Both the Si and glass substrates were first hand washed with a solution of Liquinox and rinsed with tap and then deionized water. They were then transferred to the laminar flow hood and stored under water until needed. Just prior to an evaporation, they were rinsed with purified water that had been filtered for 0.2 μm particles and then degreased and dried in acetone vapor. The leads, spacers and electrodes

consisted of deposited Pb (99.99% pure) thermally evaporated from Ta boats at a rate of 50 Å/s and a pressure of 10^{-3} Pa. Evaporations were monitored using a quartz crystal thickness monitor.

Differential capacitance and conductance were measured as a function of voltage with a standard apparatus that utilizes a current sensitive preamplifier and lock-in amplifier.[12] A 10 mV, 100 kHz modulation voltage was applied across the capacitor on top of a sweeping DC bias (sweep rate = 60 mV/sec, lock-in time constant = 3 ms).

All measurements were taken at room temperature immediately after the Pb evaporation. We, therefore, estimated that the native oxide was less than 100 Å thick on the Pb electrode. The Si wafer was stored in air for months before these measurements so that its surface had oxidized. The oxide thickness was measured with an ellipsometer and found to be 60 Å. Doping density was determined from the resistivity of the Si wafer.[13]

Figure 2 shows the measured differential capacitance versus voltage curves for the Pb-air-n type Si <111> capacitor. The insulator capacitance (V > 3 volts) was decreased by decreasing the squeezing force starting with curve a. Each curve has a capacitance step associated with the formation of an accumulation layer near the silicon surface.[13] The insulator thicknesses were estimated from the accumulation capacitances using the formula $d = \varepsilon_0 A/C$. The low depletion capacitance (< 20 pfd) and low threshold voltage (< 2 volts) are consistent with the measured doping density of 2×10^{14} cm^{-3} for curve d, the largest estimated thickness.[14] The other curves give lower

calculated doping densities possibly caused by electrode tilt or roughness that becomes more noticeable for small insulator thicknesses. In addition, hysteresis was apparent in the C-V and G-V data for faster sweep rates (> 60 mV/sec) indicating the presence of oxide surface mobile ions. The wide adjustability of the insulator capacitance, however, shows that most of the insulator is air gap.

Figure 3 shows the differential conductance versus voltage curves corresponding to the capacitance curves in Fig. 2. As previously observed for Si MOS junctions, there exist maxima near the flat band voltage indicating the presence of surface states.[14] Surface state structure is also apparent in the capacitance curves.[15] Leakage currents are apparent at higher biases possibly due to electrode tilt or roughness. These excess currents may be due to metal-semiconductor contact or tunneling through a very thin insulating gap. They are not caused by electrical discharge in the air gap since the ionization potential of air molecules is typically 10 volts, larger than the bias range used in these experiments.

The following comments summarize these preliminary results on mechanically adjustable air-gap MIS systems.

1) A variable air-gap MIS capacitor can be constructed using standard evaporation techniques and a recently developed squeezable junction geometry.[7] Care must be taken, however, to avoid dust contamination.

2) Stray capacitance and metal electrode tilt can be minimized using the proper junction geometry and squeezer design.[8]

3) The wide adjustability of the capacitance obtained for a Pb-air-n type Si <111> capacitor suggests that most of the insulator is the variable air-gap. Further investigations concerning the effects of native oxides, electrode tilt and surface roughness are necessary for a more quantitative understanding of these capacitors.

4) Surface state structure is apparent in the observed C-V and G-V data for the Pb-air-Si capacitor.

These results then raise interesting possibilities for experiments: a) on clean semiconductor surfaces, illuminating physics previously hidden by the presence of the oxide layer, b) on semiconductors' surfaces on which high quality native oxides cannot be grown and c) on semiconductor surfaces before and after deposition of insulators. It may be particularly interesting to follow the surface states through a series of processing steps on a single semiconductor surface.

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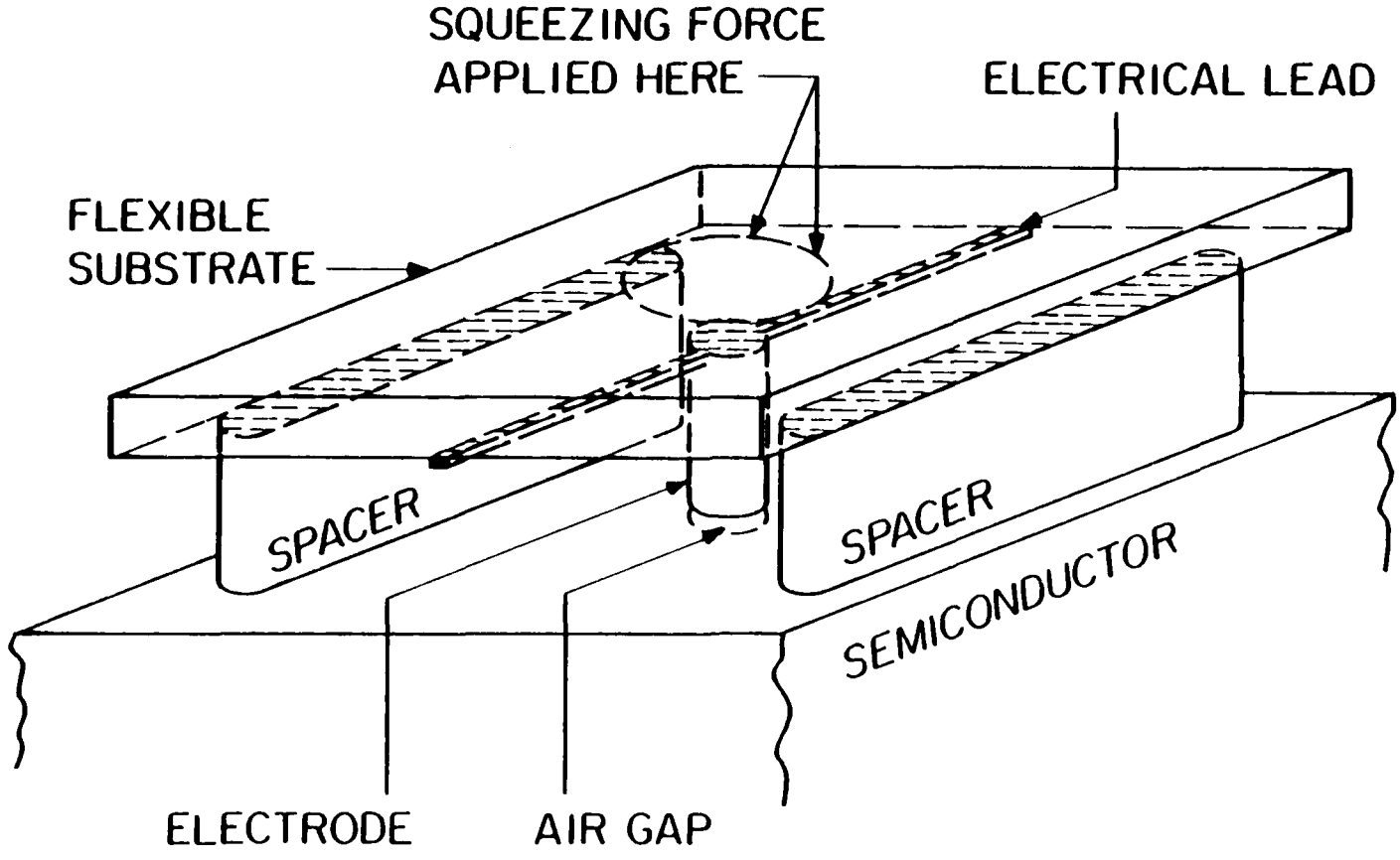
Figure Captions

Fig. 1. A schematic view of a metal-air-semiconductor capacitor. The vertical scale is distorted for clarity. Actually, the slide is ≈ 1 mm thick, the spacers are ≈ 10 μ thick, the electrical leads are ≈ 0.1 μ thick and the electrode is ≈ 9 μ thick. Thus, the electrode starts out about 1 μ above the semiconductor. It is brought nearer by applying a force to bend the glass slide. The force is applied between a 5 mm diameter, hollow cylinder centered over the electrode and a flat surface under the semiconductor.

Fig. 2. Differential capacitance versus voltage curves for various squeezing forces on a Pb-air-n type Si <111> MIS capacitor using the configuration illustrated in Fig. 1. The estimated air-gap thicknesses for curves a-d are 1700, 2200, 2900 and 3600 Å, respectively.

Fig. 3. Differential conductance versus voltage curves for various squeezing forces on a Pb-air-n type Si <111> MIS capacitor using the configuration illustrated in Fig. 1. The estimated air-gap thicknesses for curves a-d are 1700, 2200, 2900 and 3600 Å, respectively.



Moreland et al.

CAPACITANCE (pFd)
50
40
30
20
10
0
-2
-1
0
1
2
3
4
VOLTAGE (V)
n=2×10^14 cm^-3
a
b
c
d
GLASS
AIR
Si<III>
Fig. 2
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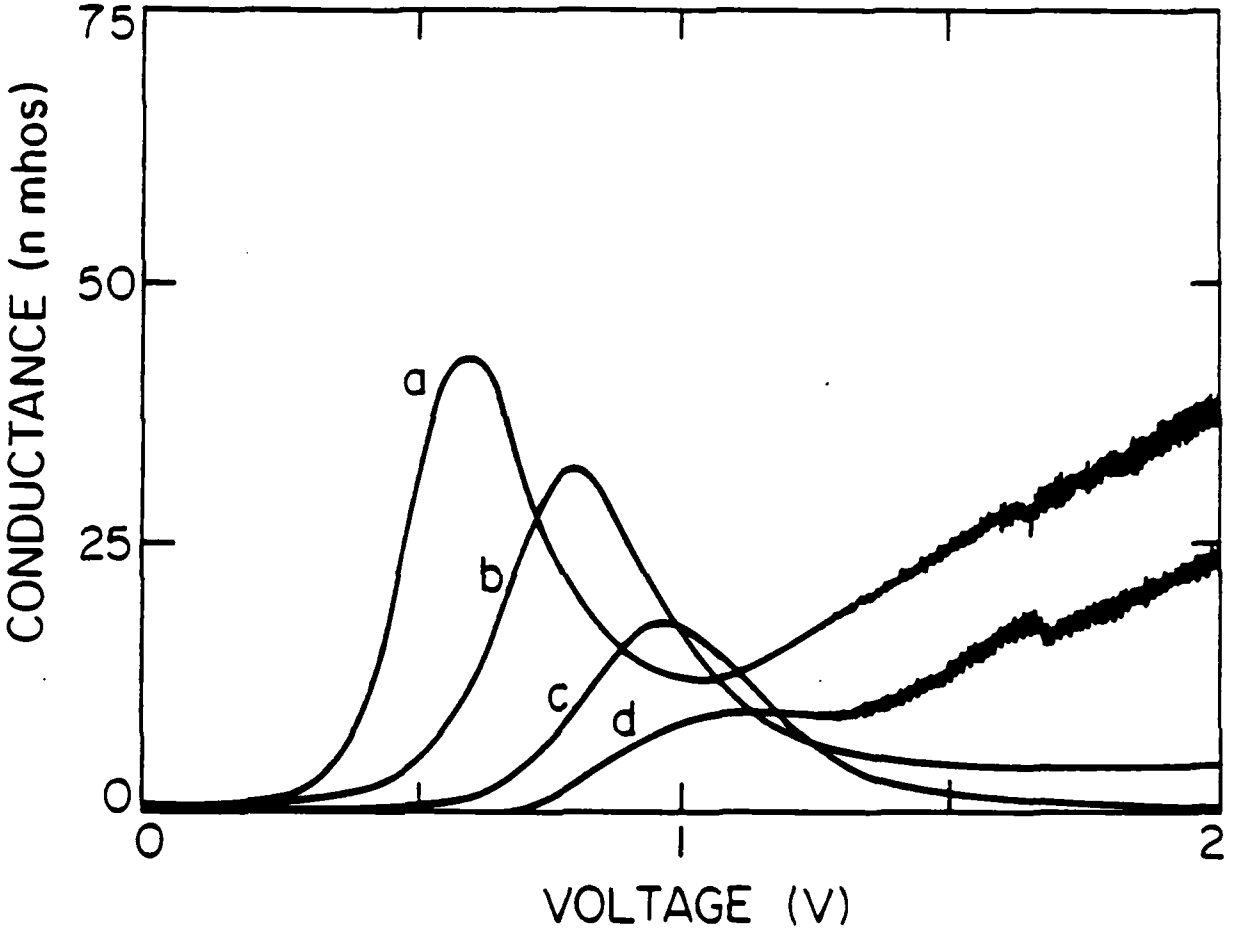

Fig. 3

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